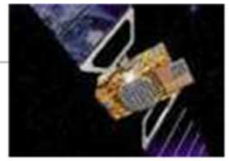
THALES

SKA (HPC workshop) 09/09/16

TRT-FR (M. BARRETEAU)






Physics Electronics

Signal, Image, Data Processing

Real Time Information Processing

Safe Information Processing

C4ISR Information Systems

Systems of systems

Reasoning and analysis in complex systems

Decision & optimization

System software engineering

Critical embedded systems

High performance computing

TRT-Fr / SKA

Scope

- Mostly: High performance real-time embedded systems (SWaP constraints)
- But also: Cloud

Useful skills and expertises

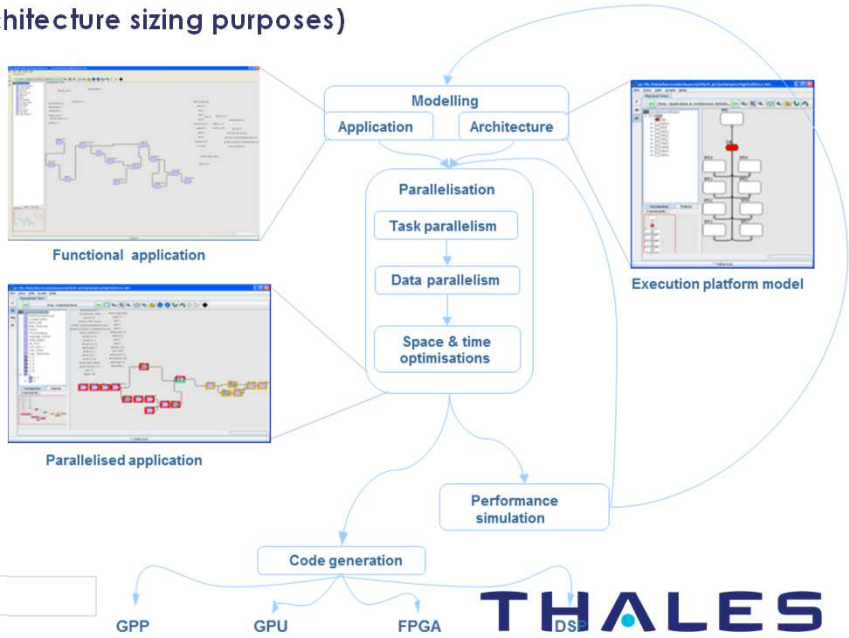
- Knowledge and design of high performance (domain-specific) parallel architectures (e.g. FPGA) with best perf/W ratio
- Parallel programming (e.g. application acceleration through a tool for mapping signal/image processing intensive computing)
- High performance and low latency network (including heterogeneous computing nodes)
- Big data, data fusion

A tooled-up approach

Programming tool for high performance real time embedded systems that face the multi/many-core era

- Goal
  - **Ease**
    - **Rapid prototyping from a high level modeling to target several heterogeneous parallel machines**
    - **Virtual prototyping (for early validation and architecture sizing purposes)**
  - **Improve productivity**
    - **Seamless design flow**
    - **Design Space Exploration**
    - **Generation of**
      - **Target parallel codes**
      - **Performance simulations**

- Support tool: SpearDE



TRT-Fr investment willingness

- "Reasonable" funding (e.g. collaborative project)
- Highly eased by some Thales operational units involvements (Thales Alenia Space)